UNIVERSITY OF COLOMBO, SRI LANKA

FACULTY OF TECHNOLOGY

LEVEL I EXAMINATION IN TECHNOLOGY - SEMESTER II - 2019

IA 1013 – COMPUTER ARCHITECTURE I

Two (02) hours

Answer four (4) questions only.

Electronic calculators are not allowed.

No. of pages: 19

Important Instructions to Candidates

- If a page or part of this question paper is not printed, please inform the supervisor immediately.
- Enter your index number on all pages of the answer script.
- Write the answers to the questions in the space provided in the question paper.
- Electronic devices capable of storing and retrieving text, including electronic dictionaries and mobile phones are not allowed.

Index No: …….....

Q	M
1	
2	
3	
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Total	

Index No:……

Answer four (04) of the five questions.

1. a). Explain each of the following terms in your own words.

(i). Data representation

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(1 mark)

(ii). Encoding

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(1 mark)

(iii). PLD

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(1 mark)

(iv). Unicode

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(1 mark)

(v). VLSI

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(1 mark)

b). How many bits is:

(i). Byte: …….. *(1 mark)*

(ii). Half-word: ……. *(1 mark)*

(iii). Word: …… *(1 mark)*

c). (i). What are the ranges of 8-bit, 32-bit, and 64-bit integers in 2's complement "unsigned" and "signed" representations?

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(6 marks)

(ii). Perform the following additions.

(A)	(B)
1101010	1100101
+1011011	+1010111
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(4 marks)

d). Perform the conversions of the fractions given in Table 1.1.

Table 1.1

Binary		**Octal**		**Hexadecimal**	
11.11_2		(i).	……	(ii).	……..
(iii).	.....	16.54_8		(iv).	……..
(v).	……	(vi).	……	$1AB.C_{16}$	

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(3 marks)

e). Convert the following numbers in IEEE single precision 32-bit floating point format into decimal numbers.

(i). 0 01111100 11100000000000000000000

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(2 marks)

(ii) 1 10000100 01110000000000000000000

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(2 marks)

2. a). State the reason to identify the NAND and NOR logic gates as universal logic gates.

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(2 marks)

b). Draw the circuit diagrams for the following Boolean functions using AND and NOT gates only.

(i). $F(X,Y,Z) = (\overline{X.Y} + Z).(\bar{Y} + Z)$

(2 marks)

(ii). $F(X,Y,Z) = \bar{X}.Y + \bar{Z}.Y$

(2 marks)

c). Evaluate the Boolean functions given below.

(i). $F(A,B,C) = (\bar{A} + B).(C + \overline{AB})$

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(3 marks)

(ii). $F(A,B,C) = \overline{(A.B) + \overline{(C + A)}}$

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(3 marks)

(iii) Find the output function and truth table for the combinational circuit logic shown in Figure 2.1.

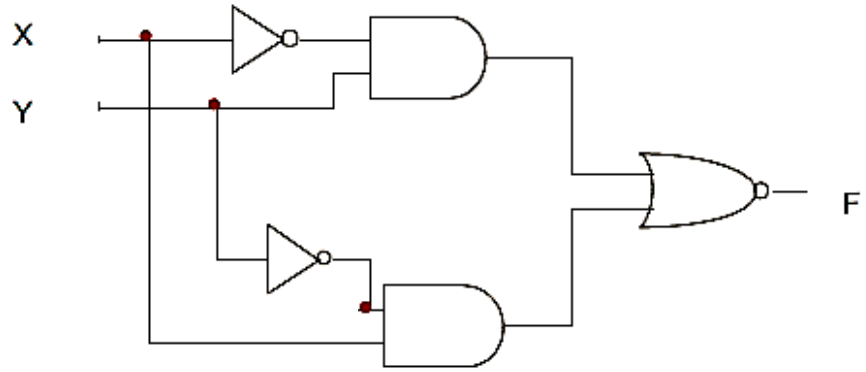

Figure 2.1

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(3 marks)

d). The sequential logic circuit contains memory elements and the output depends on the current value of input and prior input-level conditions. Figure 2.2 shows the block diagram of sequential logic. As shown in the figure, the outputs of combinational logic are the inputs to memory elements and the outputs of memory elements are the inputs to combinational logic; the basic elements of memory elements are flip-flops that can hold binary values as long as the device is powered.

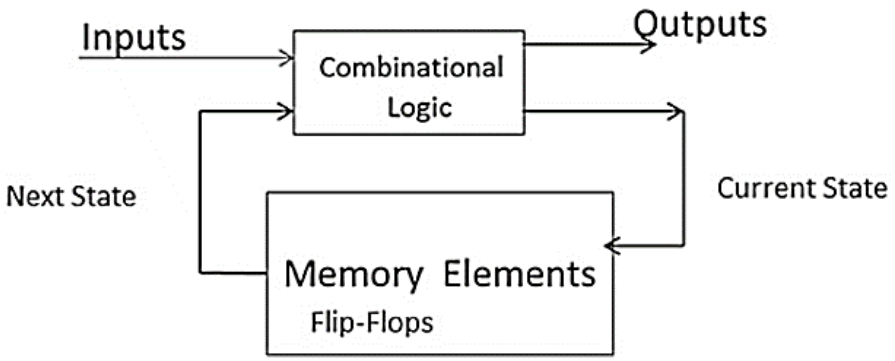

Figure 2.2

(i). Draw the circuit diagrams for the S-R and D flip-flops by using the appropriate logic gates, then show the corresponding truth tables.

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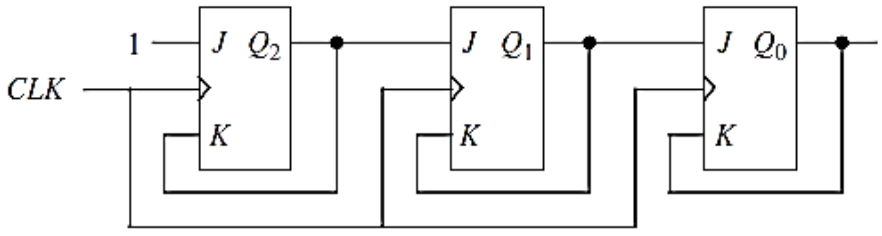
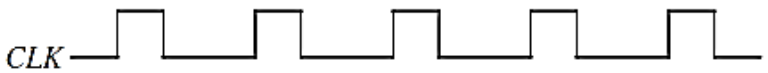
(4 marks)

(ii). The following circuit has three master-slave J-K flip-flops. There is a single input CLK and three outputs Q_2, Q_1, and Q_0 that initially have the value 0. Complete the timing diagram by showing the values for Q_2, Q_1, and Q_0. Assume that there are no delays through the flip-flops.





Q_2 ——

Q_1 ——

Q_0 ——

(6 marks)

3. a). (i). List down the components of a microcomputer.

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(4 marks)

(ii). Explain the main idea of von Neumann microcomputer design.

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(3 marks)

(iii). Distinguish between von Neumann and Harvard architectures using suitable block diagrams.

(6 marks)

b). (i). Explain the difference between a microprocessor and a microcontroller?

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(2 marks)

(ii). Is flash memory a type of RAM or ROM? Explain.

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(2 marks)

(iii). What are the write mechanism and the erasure of PROM?

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(2 marks)

d). (i). Compare and contrast PLA and PAL systems.

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(2 marks)

(iv). Implement the PLA system given in Table 3.1.

Table 3.1

X2	X1	X0	Z1	Z2
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1

(4 marks)

4. a). (i). Describe a multicore processor with the aid of a suitable block diagram.

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(3 marks)

(ii). What are the major roles that the registers perform in a processor?

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(2 marks)

(iii). What are the main stages of the processor instruction cycle?

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(3 marks)

b). (i). Briefly explain the internal structure of the CPU.

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(4 marks)

(ii). What are the elements of a machine instruction?

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(4 marks)

c). Describe the following instruction set operations.

(i). Push

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(1 mark)

(ii). Add

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(1 mark)

(iii). Jump

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(1 mark)

(iv). Halt

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(1 mark)

d). (i). Describe the function of "Data Multiplexing".

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(1 mark)

(ii). Compare and contrast Time Division Multiplexing and Frequency Division Multiplexing.

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(2 marks)

(iii). What are the application areas of Data Multiplexing techniques?

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(2 marks)

5. a). (i). What are the two major approaches to store real numbers?

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(2 marks)

(ii). Order the numbers of $(1.1)_2$, $(1.7)_8$, and $(1.5)_{10}$ from largest to smallest.

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(3 marks)

(iii). Give the values of 88, 1, 127, and 225 in 8-bit unsigned representation.

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(4 marks)

b). Simplify the following Boolean functions.

(i). $F(X,Y) = X.Y + (\bar{X}.\bar{Y})$

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(3 marks)

(ii). $F(X,Y,Z) = \overline{(X.Y)} + \overline{(X+Y+Z)}$

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(3 marks)

c). (i). Using a block diagram illustrate the basic microcontroller architecture.

(4 marks)

(ii). What are the basic features of a microcontroller?

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(2 marks)

d). Three computers which have different data transferring rates are connected to a multiplexer and their information are illustrated in Table 5.1.

Table 5.1

Computer	**Data transferring speed/Mbps**	**Data label**
C_1	45	a
C_2	0	0
C_3	15	b

Give the output data streams from the multiplexer, if the system supposed to use following multiplexing techniques.

(i). Statistical Time Division Multiplexing

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(2 marks)

(ii). Synchronous Time Division Multiplexing

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(2 marks)