

UNIVERSITY OF COLOMBO, SRI LANKA FACULTY OF TECHNOLOGY

LEVEL II EXAMINATION IN TECHNOLOGY – Semester I – 2019

IA 2003 – Computer Architecture I

Answer All Questions
Time: Two (02) hours
No. of Pages: 14
Total 100 marks

Important Instructions to Candidates

- This paper consists of 04 questions. Answer all questions.
- If a page or a part of this question paper is not printed, please inform the supervisor immediately.
- Enter your Index Number on all pages in the answers script.
- STRUCTURED ESSAY TYPE: Write the answers to these questions in the space provided in the question paper.
- Electronic devices capable of storing and retrieving text, including electronic calculators, dictionaries and mobile phones are not allowed.

Question	Marks
1	
2	
3	
4	
Total	

				Index Number:
1.	a).	Expla	ain each of the following terms in your own words.	
	,	(i).	Digitization	
		(ii).	Character code	(1 mark)
				(1 mark)
		(iii).	Mantissa	
		<i>(</i> •)	EDD 014	(1 mark)
		(1V).	EPROM	
		()		(1 mark)
		(V).	Opcode	

(1 mark)

		Inde	x Number:
b).	What	at are the two major approaches to store real numbers in mode.	rn computing?
			(2 marks)
c).	(i).	What are the ranges of 16-bit and 32-bit integers in 2' "signed" representations?	s complement "unsigned" and
			(4 marks)
	(ii).	Give the values of $+127$, 0, -127 in 8-bit sign-magnitude are representation.	nd 8-bit 1's complement signed

d). Convert the fractions given in Table 1.1 appropriately.

Table 1.1

	Binary		Octal		Decimal	Hexadecimal					
	10.112	(i).		(ii).		(iii).					
	- · · · <u>-</u>										
(iv).			13.1463 ₈		11.20 ₁₀	(v).					
	•••••						•••••				
(vi).		(vii).		(viii).			AB.11 ₁₆				

(6 marks)

			Index Number:
- \	F	and the full continuous have in IEEE 22 bit flooring main	(4 marks)
e).		ess the following numbers in IEEE 32-bit floating poin	it format.
	(i).	-7	
			/2 1

Index Number:	

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- 2. a). Draw the circuit diagrams for the following Boolean functions using only NAND gates.
 - $(i). \hspace{0.5cm} F(X,Y) = \overline{(X+Y)} + (\overline{X} + \overline{Y})$

(2 marks)

(ii). $F(X, Y, Z) = X.Y + \overline{Z}.Y$

(2 marks)

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Index Number:	

(iii).	F(X,	Y, Z	(x) = X.	(Y +	Z)	$+\overline{Y}.\overline{X}$

b).	Evalu	uate the following Boolean function and Boolean expression respectively.
	(i).	$F(A, B, C) = (\overline{A.C} + B). C$

	 																					 			. 				 	
• •	 • •	• • •	• • •	• •	• • • •		• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • •	• • • •		• • •	• • •	 • • •	• • •	• • • •		• • •	• • •	• • • •	 	
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(ii).	$(\overline{A} + \overline{B}) = \overline{A}. \overline{B}$	(3 marks)

(3 marks)

Index Number:	
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c).		cally, the sequential circuits rely on feedback in order for retaining their state valuedback in digital circuits occurs when an output is looped to the input. What is the most basic sequential logic component?	ues and,
	(ii).	Draw the circuit diagram for the above mentioned component using appropriates and show the corresponding truth table.	
			(4 1)
	(iii).	What are the applications of sequential logic circuits in computers?	(4 marks)
			•••••
			(2 marks)

d). Illustrate the function of the logic circuit shown in Figure 2.1.

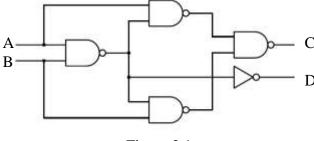


Figure 2.1

		Index Number:
		(5 marks)
3. a). (i).	What is the main idea of von Neumann microcomputer design?
		(2 marks)
(i	i).	Discuss the difference/s between von Neumann and Harvard architectures using suitable block diagrams.

			index Number:
b).	A coi	mputer memory unit stores binary information in group	os of bits called words.
	(i).	Illustrate a computer memory unit using a block diag	ram.
			(2 marks)
	(ii).	When consider the computer memory, what is the role	e of a floating gate transistor (FGT)?
			(3 marks)
	(iii).	What are the write mechanism and the erasure of RA	M?
			(2 marks)
c).		rammable Logic Device (PLD)s are used to design com and, it can be categorised into three main groups; ROI	
	(i).	What are the limitations of ROM?	

		Index Number:
(ii).	Give the meanings of "PLA" and "PAL".	
		(2 marks)
(iii).	Explain the significant difference/s between PLA and	d PAL systems.
(iv).	Implement the PLA system given in Table 3.1.	(2 marks)

Table 3.1

X2	X1	X0	Z 1	Z2
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

		Index Number:
		(6 marks)
4. a). (i).	Illustrate the structure of IAS (Institute of Advance Structure found in 1946.	udies) computer which was the first-

(ii).	What are the IAS memory formats for a number word and an instruction word?	
		(4 marks)
(iii).	What are the main stages of the processor instruction cycle?	
		• • • • • • • • • • • • • • • • • • • •
		(3 marks)
(iv).	Draw the state diagram of processor instruction cycle.	

Index Number:

(4 marks)

Index Number:	
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b).	Describe the following instruction set operations.				
	(i).	Move			
			•••••		
			(1 mark)		
	(ii).	Negate			
			•••••		
	(iii)	Pop	(1 mark)		
	(111).	тор			
			(1 mark)		
c).	(i).	Describe the function of "Data Multiplexing".			
			•••••		
			(1 mark)		
	(ii).	Compare and contrast Frequency Division Multiplexing and Wavelength Multiplexing.	Division		
			•••••		
			•••••		
			•••••		
			2 marks)		

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maex	Number:	

d). Three computers which have different data transferring rates are connected to a multiplexer and their information are illustrated in Table 4.1.

Table 4.1

Computer	Data transferring speed/Mbps	Data label
A	30	a
В	0	0
С	20	b

Give the output data streams from the multiplexer, if the system supposed to use following multiplexing techniques.

(i).	Synchronous Time Division Multiplexing				
(ii).	Statistical Time Division Multiplexing (2 marks)				
	(2 marks)				